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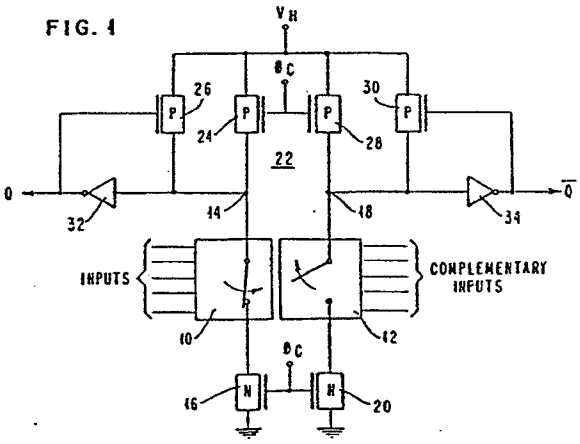
(54) **Clocked differential cascode voltage switch logic systems.**

(57) A clocked differential cascode voltage switch (CVS) logic system is provided for a complete logic family which has a first switching circuit (10) that produces a given output signal at a first output node (14) and a second switching circuit (12) that produces a second output signal which is the complement of that of the given output signal at a second output node (18). First and second clocked devices (24, 28) are connected from the first and second output nodes (14, 18), respectively, to a voltage source (V_H), the first and second inverters (32, 34) are connected to the first and second output nodes (14, 18), respectively. Additionally, a regenerative circuit (26, 30) may be connected between the first and second output nodes (14, 18) and the voltage source (V_H).

FIG. 1



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CLOCKED DIFFERENTIAL CASCODE VOLTAGE SWITCH LOGIC SYSTEMS

This invention relates to logic systems and more particularly to differential logic systems of the cascode voltage switch (CVS) type.

Logic systems of the single ended cascode voltage switch type are described in commonly assigned U. S. Patent Application having Serial No. (BU9-83-021) filed by W. R. Griffin and L. G. Heller on even date. These circuits are generally made in the complementary metal oxide semiconductor (CMOS) technology having an N channel transistor, or NMOS, matrix as a logic system with a P channel transistor, or PMOS, matrix as a complementary logic network.

Another of the cascode voltage switch type logic circuits, but of a differential type, is disclosed in commonly assigned U. S. Patent Application Serial No. 508,454, filed by J. W. Davis and N. G. Thoma on June 27, 1983. This differential logic circuit includes cross-coupled P channel load devices coupled to complementary outputs of an NMOS logic network.

In an article in 1981 IEEE International Solid-State Circuits Conference, February 20, 1981, pp. 230, 231 and 276 by B. T. Murphy et al entitled "A CMOS 32b Single Chip Microprocessor" and also in an article in IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 3, June 1982, by R. H. Krambeck et al entitled "High-Speed Compact Circuits with CMOS" there is disclosed single-ended clocked dynamic CMOS logic circuits which include a P channel device as a load connected to an NMOS logic network with an inverter

connected between an output terminal and the P channel load device.

It should be noted that the above referenced Murphy et al and Krambeck et al logic circuits cannot be used to provide a complete logic family.

It is an object of this invention to provide a logic circuit which produces a complete logic family with differential outputs and which is free of output skew and glitching.

In accordance with the teachings of this invention, a differential logic system is provided which has a first switching circuit that produces a given output signal at a first output node and a second switching circuit that produces a second output signal which is the complement of that of the given output signal at a second output node. First and second clocked devices are connected from the first and second output nodes, respectively, to a voltage source, and first and second inverters are connected to the first and second output nodes, respectively. Additionally, a regenerative circuit may be connected between the first and second output nodes and the voltage source.

The foregoing and other objects, features and advantages of the invention will be apparent from the following and more particular description of the preferred embodiments of the invention, as illustrated in the accompanying drawings in which

Fig. 1 illustrates one embodiment of the present invention as a clocked differential CVS logic system made in CMOS technology,

Fig. 2 illustrates another embodiment of the present invention as a clocked differential CVS logic system made in NMOS technology, and

Fig. 3 shows an exclusive OR circuit in the system of the present invention made in CMOS technology.

Referring to the drawings in more detail, there is illustrated in Fig. 1 one embodiment of the present invention which is a clocked differential cascode voltage switch logic circuit or system that includes first and second logic networks 10 and 12 each acting as a switch such that when one of the switches is closed, such as 10, the other switch 12 is open, and vice versa. Given input signals, identified as inputs, and input signals complementary to the given input signals, identified as complementary inputs, are applied to first and second logic systems 10 and 12, respectively, for controlling the operation of the switches in systems 10 and 12. Network 10 is connected between an output node 14 and one electrode of a first enabling or pull down N channel transistor 16 and network 12 is connected between an output node 18 and one electrode of a second enabling N channel transistor 20. A clock pulse ϕ_C is applied to the control gates of transistors 16 and 20 with the other electrodes of these transistors being connected to ground.

A load circuit 22 includes first and second P channel transistors 24 and 26 connected between output node 14 and a source of potential V_H which may have a voltage of +5 volts. The load circuit 22 also includes third and fourth P channel transistors 28 and 30 connected between output node 18 and source V_H. The clock pulse

ϕ_C is also applied to the control gates of transistors 24 and 28. An inverter 32 is connected between output node 14 and an output terminal Q, with the output terminal Q being connected to the control gate of transistor 26. An inverter 34 is connected between output node 18 and an output terminal $\bar{Q}$, with the output terminal Q being connected to the control gate of transistor 30.

In the operation of the system of Fig. 1, the output nodes 14 and 18 are precharged to +5 volts by applying a low voltage with clock pulse ϕ_C to the control gates of the transistors 24 and 28 which turn on the transistors 24 and 28. During precharge time both output terminals Q and $\bar{Q}$ are at a low voltage and, therefore, all inputs to the logic networks 10 and 12 from other similar systems are also low at this time. To evaluate the information applied to inputs and complementary inputs of logic networks 10 and 12, respectively, the clock pulse ϕ_C applies a high voltage to enabling transistors 16 and 20 which turns on transistors 16 and 20, transistors 24 and 28 being turned off. In view of the dual nature of the first and second networks 10 and 12, one of these networks will act as a closed switch, e.g., network 10, which effectively grounds output node 14, while network 12 acts as an open switch which prevents output node 18 from discharging.

Since the voltage at output node 18 is high at approximately +5 volts, the voltage at the output terminal $\bar{Q}$ is low due to the presence of the inverter 34. With the voltage at the output terminal $\bar{Q}$ low, the P-channel transistor 30 is turned on to maintain the voltage at output node 18 at +5 volts. Similarly, it can be seen that with the voltage on the output node 14 low, the voltage on the output terminal Q is high which main-

tains the P channel transistor 26 in an off condition. As can be seen, if desired, a single N channel transistor may be used instead of the two transistors 16 and 20.

It can be readily seen that with the complementary input signals, inputs and complementary inputs, applied to the first and second networks 10 and 12, respectively and with inverters 32 and 34 connected to differential output terminals Q and $\bar{Q}$ any logic function can be performed in the system of Fig. 1, i.e., the system of Fig. 1 is capable of providing a complete clocked logic family.

The embodiment of the invention illustrated in Fig. 2 of the drawings is similar to that of Fig. 1 with the principal difference being the use of N channel transistors for the load, indicated by 22', in place of the P channel transistors 24, 26, 28 and 30.

The clocked N channel transistor of the load 22' include transistors 24' and 28' having a clock pulse $\bar{\phi}_C$ applied to the control gates thereof. The feedback transistors of load 22' include N channel transistors 30' and 26' with the output terminal Q being connected to the control gate of the transistor 30' and the output terminal $\bar{Q}$ being connected to the control gate of the transistor 26'. The logic network of the circuit of Fig. 2 of the drawings may be represented by a single network 10',12' which functions in much the same manner as the dual networks 10 and 12 of the logic system of Fig. 1, i.e., with differential inputs applied to the logic network 10',12' and enabling N channel transistor 16',20' turned on by clock pulse ϕ_C only one of the

nodes 14 and 18 are connected to ground during any given instant of time.

In the operation of the logic system of Fig. 2 of the drawings, the output nodes 14 and 18 are precharged to approximately +5 volts by applying a high voltage with clock pulse $\bar{\phi}_C$ to the control gates of the transistors 24' and 28' which turns on the transistors 24' and 28'. To now evaluate the information applied to the differential inputs of the logic network 10',12', the clock pulse $\bar{\phi}_C$ goes to a low value turning off the transistors 24' and 28' and the voltage of clock pulse ϕ_C rises to turn on the enabling transistor 16',20'. In view of the dual nature of the switching arrangement in the logic network 10',12', one of the switching paths in network 10',12' closes to discharge, e.g., node 14 through the enabling transistor 16',20' to ground, while the other switching path remains open, preventing node 18 from discharging.

Since the voltage at the output node 18 is high, the voltage at the output terminal Q is low due to the presence of the inverter 34. With the voltage at the output terminal Q low, the feedback transistor 30' is off, preventing charge from flowing to the node 14. Similarly, it can be seen that with the voltage on the output node 14 low, the voltage on the output terminal $\bar{Q}$ is high which maintains the transistor 26' on, charging node 18 to approximately +5 volts. It should be noted that the NMOS logic system of Fig. 2 requires two clock pulses, ϕ_C and $\bar{\phi}_C$, whereas the CMOS logic system of Fig. 1 requires only one clock pulse, ϕ_C.

Fig. 3 of the drawings illustrates the logic system of the present invention of the CMOS type shown in Fig. 1

with an exclusive OR logic network 10',12' made of N channel transistors N and the PMOS load with a first inverter 32' including a P channel transistor 32A and an N channel transistor 32B and a second inverter 34' including a P channel transistor 34A and an N channel transistor 34B. This exclusive OR circuit may be expressed by the Boolean function

$$Q = \bar{A}BCD + A\bar{B}CD + AB\bar{C}D + ABC\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}C\bar{D} + \bar{A}\bar{B}\bar{C}D.$$

By referring to the Boolean function Q, it can be seen that, e.g., if the first product or term $\bar{A}BCD$ has each literal represented by a binary 1, i.e., a high voltage, transistors 36, 38, 40 and 42 in the exclusive OR network 10',12' turn on to provide a discharge path from node 14 to ground through the enabling N channel transistor 16',20'. Thus, the output terminal Q will be high or representative of a 1 binary digit of information. It should be noted that under these conditions there is no conductive path to ground from node 18, thus, node 18 remains high turning on inverter transistor 34B while inverter transistor 34A is off and output terminal $\bar{Q}$ is at a low voltage.

Likewise, it can be seen that any of the other terms or products of the Boolean function Q will produce a 1 binary digit, or high voltage, at output terminal Q when each of their literals is represented by a 1 binary digit or a high voltage, with output terminal $\bar{Q}$ being low.

Although a differential 4-way exclusive OR circuit is shown as the logic network 10',12' in Fig. 3 of the

drawings, it should be understood that any logic circuit, such as a NAND or NOR circuit, of a complete family of logic circuits may be used in logic network 10',12' with differential outputs provided at output terminals Q and $\bar{Q}$. It should also be understood that the CVS logic system of the present invention provides a complete clocked logic family which is glitch-free with high performance. Additionally, the system of the present invention does not develop an output skew problem since output nodes 14 and 18 are never pulled up during an evaluation, only during the precharge period.

To more completely describe the invention, CMOS systems as well as an all NMOS system have been illustrated, however, it should be noted that for most applications the CMOS system is preferred since it does not require two clock pulse sources, as does the NMOS system.

C L A I M S

1. Clocked differential cascode voltage switch logic system, characterized by

a first switching circuit (10) including input terminals (INPUTS) and a first output terminal (14) having a given signal,

a second switching circuit (12) including input terminals (COMPLEMENTARY INPUTS) and a second output terminal (18) having a signal complementary to that of said first output terminal (14),

a voltage source (V_H),

a first clocked device (24) connected between said voltage source (V_H) and said first output terminal (14),

a second clocked device (28) connected between said voltage source (V_H) and said second output terminal (18),

a first inverter circuit (32) connected to said first output terminal (14),

a second inverter circuit (34) connected to said second output terminal (18), and

means for applying logic signals simultaneously to the input terminals of said first and second switching circuits (10 and 12).

2. Logic system as set forth in claim 1 characterized by including clocked enabling means (16, 20) connected between each of said first and second switching circuits (10, 12) and a point of reference potential and means for simultaneously applying clocked pulses to said first and second clocked devices (24, 28) and to said clocked enabling means (16, 20).

3. Logic system as set forth in claim 1 or 2 characterized by including feedback circuits (26, 30) connected between said first and second output terminals (14, 18) and said voltage source (V_H).

4. Logic system as set forth in claim 3 characterized by including a first P or N channel feedback transistor (26) connected in parallel with said first clocked device (24) having a control gate connected to the output of said first inverter (32) and a second P or N channel feedback transistor (30) connected in parallel with said second clocked device (28) having a control gate connected to the output of said second inverter (34).

5. Logic system as set forth in claims 1 to 4, characterized in that said first inverter circuit (32) includes a first P channel transistor (32A) and a first N channel transistor (32B) serially interconnected between said voltage source (V_H) and a point of reference potential with the control gates of each of said transistors being connected to said first output terminal (14), and said second inverter circuit (34) includes a second P channel transistor (34A) and a second N

channel transistor (34B) serially interconnected between said voltage source (V_H) and said point of reference potential with the control gates of each of said second P and N transistors being connected to said second output terminal (18).

6. Logic system as set forth in claims 1 to 5, characterized in that said clocked devices (24, 28) are either P channel or N channel devices and that means are included for applying clocked pulses (C) simultaneously to the control gates of said devices.

7. Logic system as set forth in claims 1 to 6, characterized in that each of said first and second clocked devices (24, 28) includes a P channel transistor and said clocked enabling means (16, 20) includes an N channel transistor.

8. Logic system as set forth in claims 1 to 6, characterized in that each of said first and second clocked devices (24, 28) and said clocked enabling means (16, 20) includes an N channel transistor.

9. Logic system as set forth in claims 1 to 8, characterized in that said first and second switching circuits (10, 20) are arranged in the form of an exclusive OR circuit.

FIG. 1

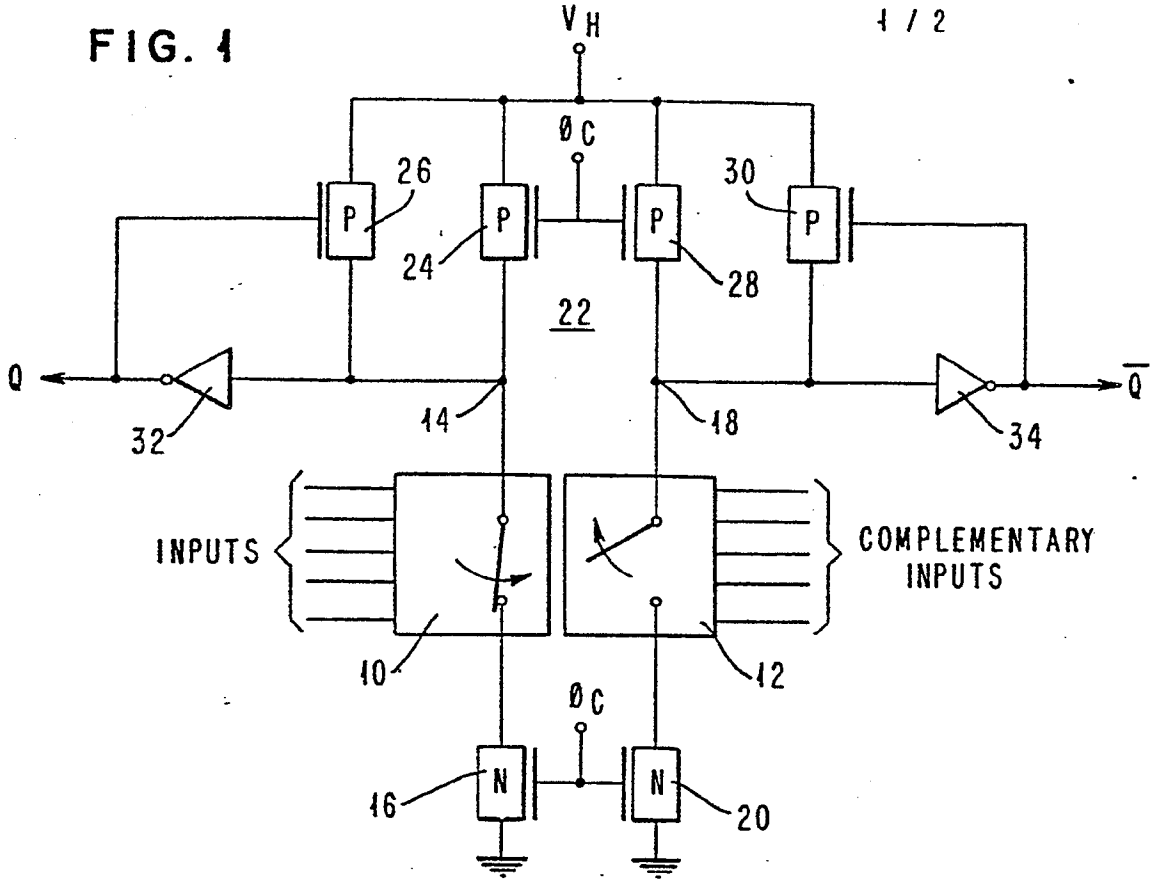


FIG. 2

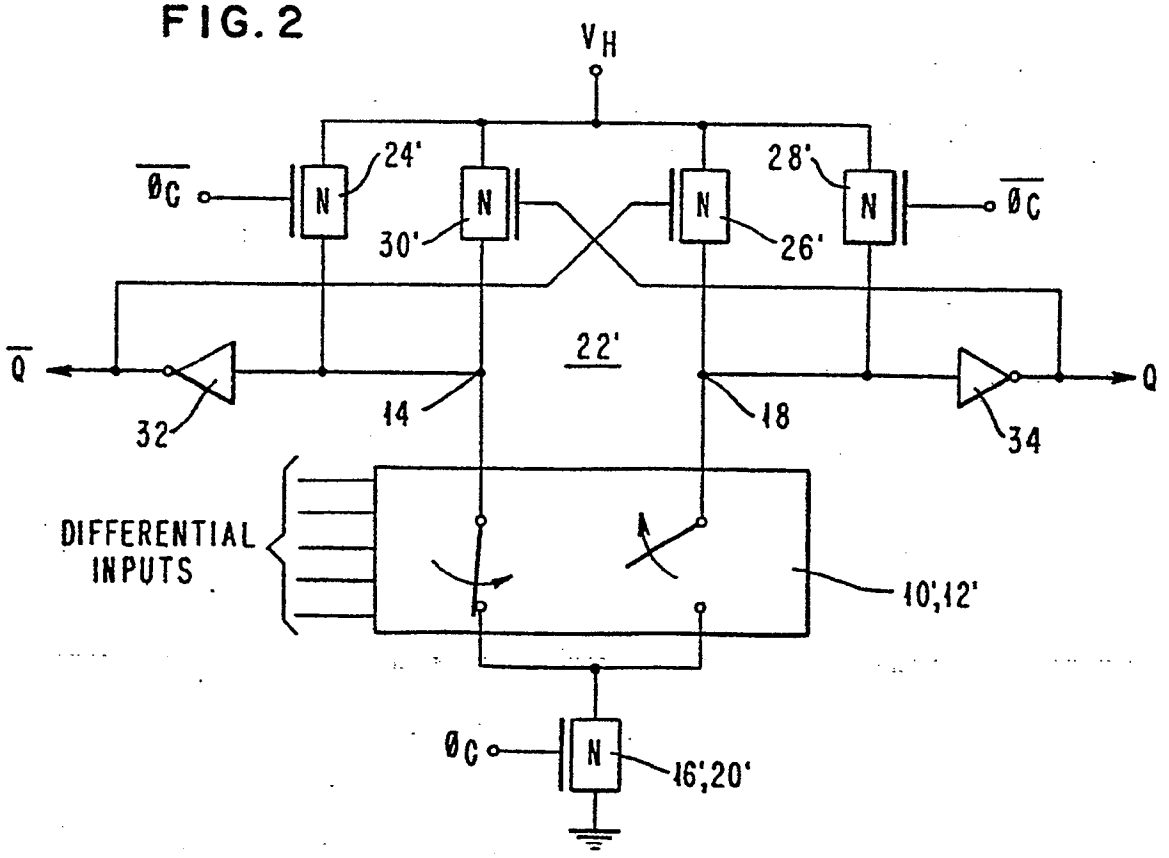
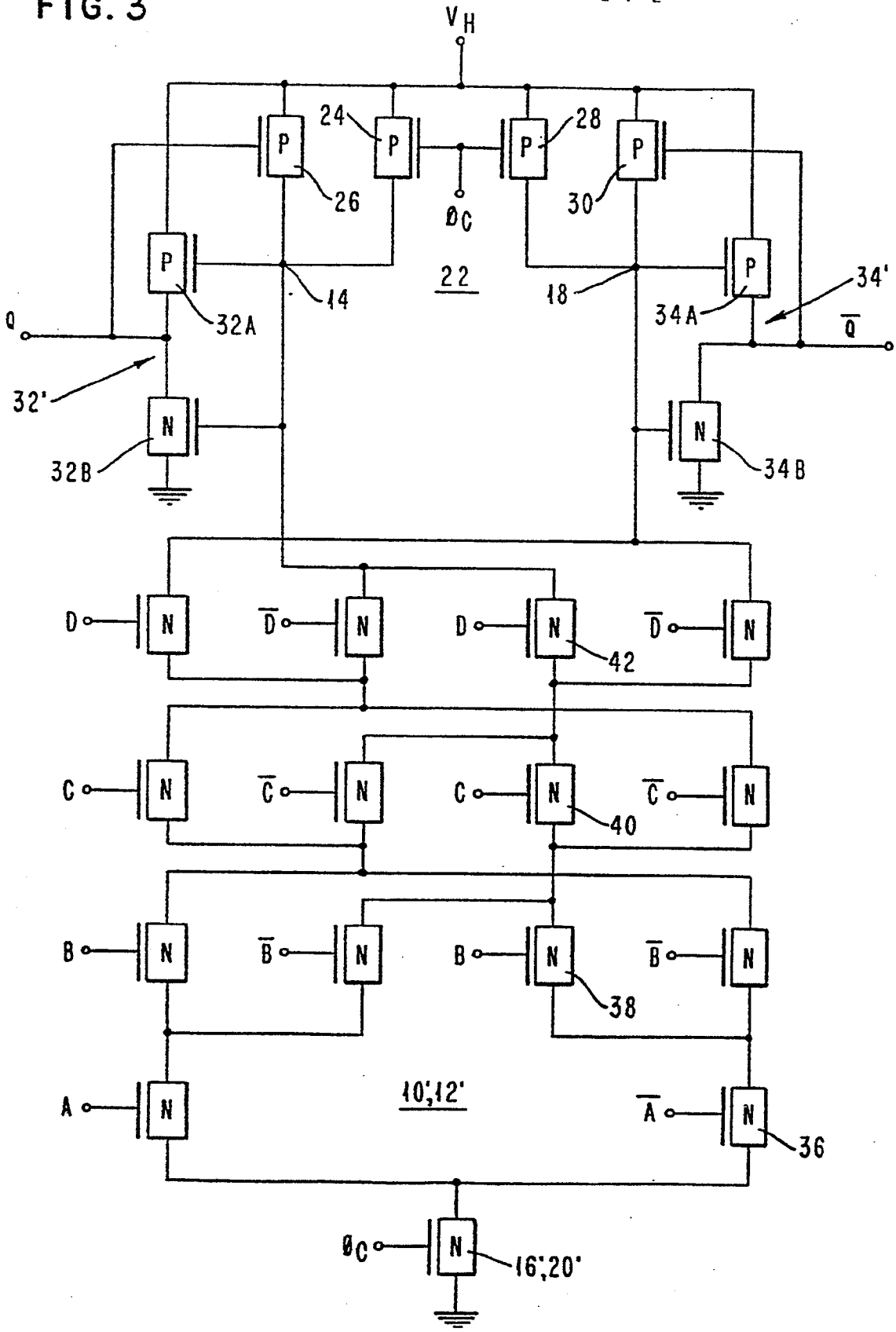


FIG. 3



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EUROPEAN SEARCH REPORT

0147598 Application number

EP 84 11 3734

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. ³)
P,X	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 26, no. 11, April 1984; T.C. LO "Non-complementary clocked differential cascode voltage switch logic", pages 6209,6210 * Complete document *	1	H 03 K 19/096
P,A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 27, no. 1B, June 1984; C.K. ERDELYI et al. "Single-ended cascode voltage switch", pages 674,675 * Figure 2 *		
A	US-A-4 367 420 (R.C. FOSS et al.)		

TECHNICAL FIELDS SEARCHED (Int. Cl. ³)

H 03 K 3/356
H 03 K 19/096
H 03 K 19/21

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	15-02-1985	ARENDT M

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